Abstract of Disclosure

In an image processing circuit, an area determination section comprises a device having a rewritable circuit configuration such as a field programmable gate array (FPGA). Consequently, the circuit configuration of the area determination section is rewritten, so that the image processing algorithm is changed. Specifically, in the area determination section, a filtering circuit and line memories (for example, FIFO memories) for forming a pixel matrix are formed by using the FPGA, and the configuration of the line memories (the lateral size and the number of lines) and the configuration of the filtering circuit are changed in accordance with a set image processing condition such as the output size or the mode.